WHAT IS CLAIMED IS:

1. A method of fabricating a semiconductor device, comprising:

forming a plurality of trench masks on a semiconductor substrate;

etching the semiconductor substrate to form trenches therein which define an active region, using the trench masks as an etch mask, the trenches and the trench masks defining a gap region;

filling the gap region with a gap fill insulating layer;

patterning the trench masks and the gap fill insulating layer until a top surface of the active region is exposed to form a trench mask pattern and a gap fill insulating pattern, which define a slit-type opening extending across the active region;

forming a gate pattern in the slit-type opening;

removing the trench mask pattern to form a contact opening exposing the active region; and

forming a contact plug to fill the contact opening.

2. The method as claimed in claim 1, wherein the trench mask is formed of a material having an etch selectivity with respect to the gap fill insulating layer.

3. The method as claimed in claim 1, wherein the trench mask is formed of a silicon nitride layer.

4. The method as claimed in claim 1, wherein the etching process for forming the trench is performed using an anisotropic etching process.

5. The method as claimed in claim 1, before forming the gap fill insulating layer, further comprising:

forming a trench oxide layer to cover inner walls of the trench; and

forming a liner layer on the surface of the semiconductor substrate including the trench oxide layer.

6. The method as claimed in claim 5, wherein the trench oxide layer is formed using thermal oxidation.

7. The method as claimed in claim 5, wherein the liner layer is formed of a silicon nitride layer.

8 The method as claimed in claim 1, wherein forming the gap fill insulating layer comprises:

forming an insulating layer on the surface of the semiconductor substrate where the trench is formed to fill the gap region bounded by the trench and the trench masks; and

planarizing the insulating layer until the trench mask is exposed.

9. The method as claimed in claim 8, wherein the insulating layer is a multiple layer formed through plural stacking and etching processes.

10. The method as claimed in claim 1, wherein the gap fill insulating layer comprisesa silicon oxide layer formed using chemical vapor deposition or spin coating.

11. The method as claimed in claim 1, wherein forming the slit-type opening comprises etching the gap fill insulating layer and the trench mask using an anisotropic etching process until the top surface of the active region is exposed.

12. The method as claimed in claim 1, wherein the slit-type opening is formed such that a top surface of the gap fill insulating pattern formed in the trench is as high as the top surface of the active region.

13. The method as claimed in claim 1, before forming the slit-type opening, further performing an ion implantation process for forming a well in the semiconductor substrate.

14. The method as claimed in claim 1, before forming the contact plug, further performing an ion implantation process for forming a source/drain in the active region which is exposed via the contact opening.

15. The method as claimed in claim 1, before forming the gate pattern, further forming a gate spacer on sidewalls of the slit-type opening.

16. The method as claimed in claim 15, wherein the gate spacer is formed of a material having an etch selectivity with respect to the trench mask pattern.

17. The method as claimed in claim 1, before forming the contact plug, forming opening spacers on sidewalls of the contact opening.

18. The method as claimed in claim 17, before forming the opening spacer, further performing an isotropic etching process for increasing the width of the contact opening.

19. The method as claimed in claim 1, wherein the contact plug is formed of a conductive material layer containing silicon atoms using epitaxial growth.

20. The method as claimed in claim 1, wherein forming the contact plug comprises:

forming a contact plug conductive layer to fill the contact opening; and

planarizing the contact plug conductive layer until a top surface of the gap fill insulating layer is exposed.

21. The method as claimed in claim 1, wherein forming the gate pattern comprises:

forming a gate insulating layer on the active region which is exposed via the slit-type opening;

forming a gate conductive pattern to fill a bottom region of the slit-type opening where the gate insulating layer is formed; and

forming a capping insulating pattern to fill a top region of the slit-type opening where the gate conductive pattern is formed, wherein the gate conductive pattern has a top surface substantially lower than those of the trench mask pattern and the gap fill insulating pattern.

22. The method as claimed in claim 21, wherein the gate insulating layer is a silicon oxide layer formed using thermal oxidation.

23. The method as claimed in claim 21, wherein the gate conductive pattern is formed of at least one selected from the group consisting of polysilicon and a metal.

24. The method as claimed in claim 21, wherein the capping insulating pattern is formed of a material having an etch selectivity with respect to the trench mask pattern.

25. The method as claimed in claim 21, before forming the capping insulating pattern, further comprising:

forming a gate interlayer insulating layer to conformally cover the inner walls of the slit-type opening where the gate conductive pattern is formed;

forming a gate upper conductive layer on the surface of the semiconductor substrate including the gate interlayer insulating layer, to fill the slit-type opening; and

etching back the gate upper conductive layer to form a gate upper conductive pattern which has a lower top surface than those of the trench mask pattern and the gap fill insulating pattern.

26. The method as claimed in claim 25, wherein the gate interlayer insulating layer is an oxide-nitride-oxide layer.

27. The method as claimed in claim 25, wherein the gate upper conductive layer is formed of a polysilicon layer and a silicide layer, which are sequentially stacked.

28. The method as claimed in claim 21, wherein forming the gate conductive pattern comprises:

forming a gate conductive layer on the surface of the semiconductor substrate including the gate insulating layer, to fill the slit-type opening; and

etching back the gate conductive layer until the top surface of the gate conductive layer becomes lower than a top of the slit-type opening.

29. The method as claimed in claim 1, wherein the gate pattern is covered with a material having an etch selectivity with respect to the trench mask pattern.

30. A semiconductor substrate comprising:

a semiconductor substrate where a trench for defining an active region is formed;

a gap fill insulating pattern filled in the trench and having a contact opening exposing the active region; and

a contact plug formed in the contact opening and connected to the active region, wherein the contact opening is a rectangular parallelepiped vacancy.

31. The device as claimed in claim 30, wherein the gap fill insulating pattern comprises a silicon oxide layer.

32. The device as claimed in claim 30, further comprising a gate pattern disposed in the slit-type opening extending across the active region and the trench, wherein the slit-type opening is bounded by the gap fill insulating pattern and the contact plug.

33. The device as claimed in claim 32, wherein the top surface of the gate pattern is as high as the top of the gap fill insulating pattern.

34. The device as claimed in claim 32, wherein the gate pattern is a gate insulating layer, a gate conductive pattern and a capping pattern, which are sequentially stacked.

35. The device as claimed in claim 34, wherein the capping pattern has substantially the same chemical composition as the gap fill insulating pattern.

36. The device as claimed in claim 32, further comprising gate spacers disposed on sidewalls of the gate pattern to separate the gate pattern from the contact plug and the gap fill insulating pattern.

37. The device as claimed in claim 34, further comprising a gate interlayer insulating layer and a gate upper conductive pattern, which are sequentially stacked, between the gate conductive pattern and the capping pattern.

38. The device as claimed in claim 37, wherein the gate interlayer insulating layer is an oxide-nitride-oxide layer.

39. The device as claimed in claim 37, wherein the gate interlayer insulating layer further has a sidewall extension that covers sidewalls of the gate upper conductive pattern.

40. The device as claimed in claim 34, wherein the gate conductive pattern is formed of at least one of polysilicon and a metal.

41. The device as claimed in claim 30, wherein the contact plug is one of an epitaxial silicon layer and a polysilicon layer.

42. The device as claimed in claim 30, further comprising opening spacers disposed between sidewalls of the contact opening and the contact plug.

43. The method as claimed in claim 30, further comprising an epitaxial silicon layer or a SOG layer at the bottom of the trench.

44. The method as claimed in claim 1, further comprising forming an epitaxial silicon layer or a SOG layer at the bottom of the trench.